REMARKS / ARGUMENTS

Claims1-15 remain pending in this application. New claims 13-15 have been added. No claims have been canceled or withdrawn.

Priority

Applicants request acknowledgment of the claim for priority in this case. The priority document was filed at the International Phase and were forwarded to the National Phase upon filing.

Abstract

The Abstract has been rewritten into better form and reduced in length.

35 U.S.C. §§102 and 103

Claims 1-2 and 4-9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Davis (U.S. Patent No. 5,805,712). Claims 10-12 stand rejected under 35 U.S.C. §102(b) as being anticipated by Nagel (U.S. Patent No. 5,592,549). Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Davis in view of Hartman (U.S. Patent No. 5,224,166). Claims 1-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the International Preliminary Examination Report (IPER).   These rejections are traversed as follows.

8

Appl. No. 09/889,410
Amendment dated February 28, 2005
Reply to Office Action of November 29, 2004

H-996

Independent claims 1, and 10 have been amended to more clearly distinguish the present invention over the cited art. For example, claims 1 and 10 have been amended to recite that the processing device deletes the key information in the single semiconductor chip if an abnormality is detected. Dependent claim 9 has been amended to recite that a power supply to the volatile memory is stopped so as to delete the key information in the single semiconductor chip if the abnormality is detected. These features that have been added to claims 1 and 10 are clearly supported by the detailed description of Fig. 8 and the volatile memory recited in claim 9 is supported by SRAM 804 in Fig. 8, for example.

Davis discloses a semiconductor means for internally decrypting input information and encrypting output information and includes processing means for processing the input and output information within the semiconductor means. A non-volatile memory is provided for storing a uniquely designated key pair used for decrypting the input information and encrypting the output information. A random numbered generator generates values used to produce at least one key internally within the semiconductor means. As such, Davis discloses that the processing device is integrated on a single semiconductor chip, internally generates key information, and internally encrypts sensitive information by the generated key information. Davis also discloses that the uniquely designated key pair is stored in a nonvolatile memory.

However, Davis does not disclose that the uniquely designated key pair is deleted if an abnormality is detected. As such, Davis fails to disclose an important feature of the presently claimed invention.

Hartman discloses a central processor that acts as a segment of both the non-encrypted and encrypted data and instructions from an external memory and causes an interface circuit to employ a decrypted master key to decrypt data and instructions from an external memory and to store the same in an internal memory cache (see column 3, lines 50-57). ROMs 32 and 34 in CPU chip 30 stores keys but not keys that are generated in CPU chip 30. Therefore, Hartman does not disclose that the processing device internally generates key information as in the presently claimed invention. In addition, the key stored in ROMs 32 and 34 cannot be deleted. As such, Hartman also fails to disclose an important feature of the present invention of deleting the key information if an abnormality is detected.

Furthermore, Hartman discloses a central processor that accesses segments of both non-encrypted and encrypted data and instructions from an external memory and causes the interface circuit to employ a decrypted master key to decrypt data and instructions from the external memory and store this information in the internal memory cache while non-encrypted data and instructions are directly stored in the internal memory cache. Therefore, Hartman discloses that the central processor inputs both encrypted and non-encrypted data and instructions from bus 44, but does not disclose that the central processor outputs both non-encrypted and encrypted data and instructions to the bus. Therefore, Hartman fails to disclose that

10

information not requiring encryption is output onto the bus to an external bus
controller.

Nagel et al disclose a control device for selecting information to be retrieved
from a secure information source, an information retrieval device such as a magnetic
storage or CD-ROM reader, coupled to the control device for retrieving the selected
information from the secure information source, and the decryption device such as a
DES integrated circuit and its related circuitry for decrypting at least portions of the
selected information retrieved from the secure information source (see column 3,
lines 30-40). While Nagel et al disclose a decryption controller which controls the
decryption key for an item from key rules and key data that are available locally, the
method of determining this key is unimportant to the present invention.
Nevertheless, Nagel et al fail to disclose that the disk system controller internally
generates key information in a single semiconductor chip and that the processing
device deletes the key information in the single semiconductor chip if an abnormality
is detected.

None of the remaining references disclose the above-mentioned features of
the present invention. In particular, it is submitted that the amendments to the claims
avoids any rejection based upon comments in the International Preliminary
Examination Report (IPER).   Furthermore, Applicants wish to clarify that document
10-275115 was not cited in the IPER, but was instead discussed in the present
specification.   It is submitted that the pending claims are patentable over this
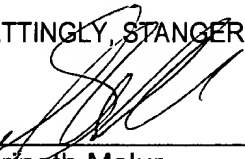
Appl. No. 09/889,410
Amendment dated February 28, 2005
Reply to Office Action of November 29, 2004

H-996

document as well.   As such, it is submitted that the pending claims patentably define

the present invention over all of the cited art.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of

Allowance be issued in this case.

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.

By

Shrinath Malur
Reg. No. 34,663
(703) 684-1120